

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : VCC
LAYER 6 : BOT

VCC_CORE

+1.5V

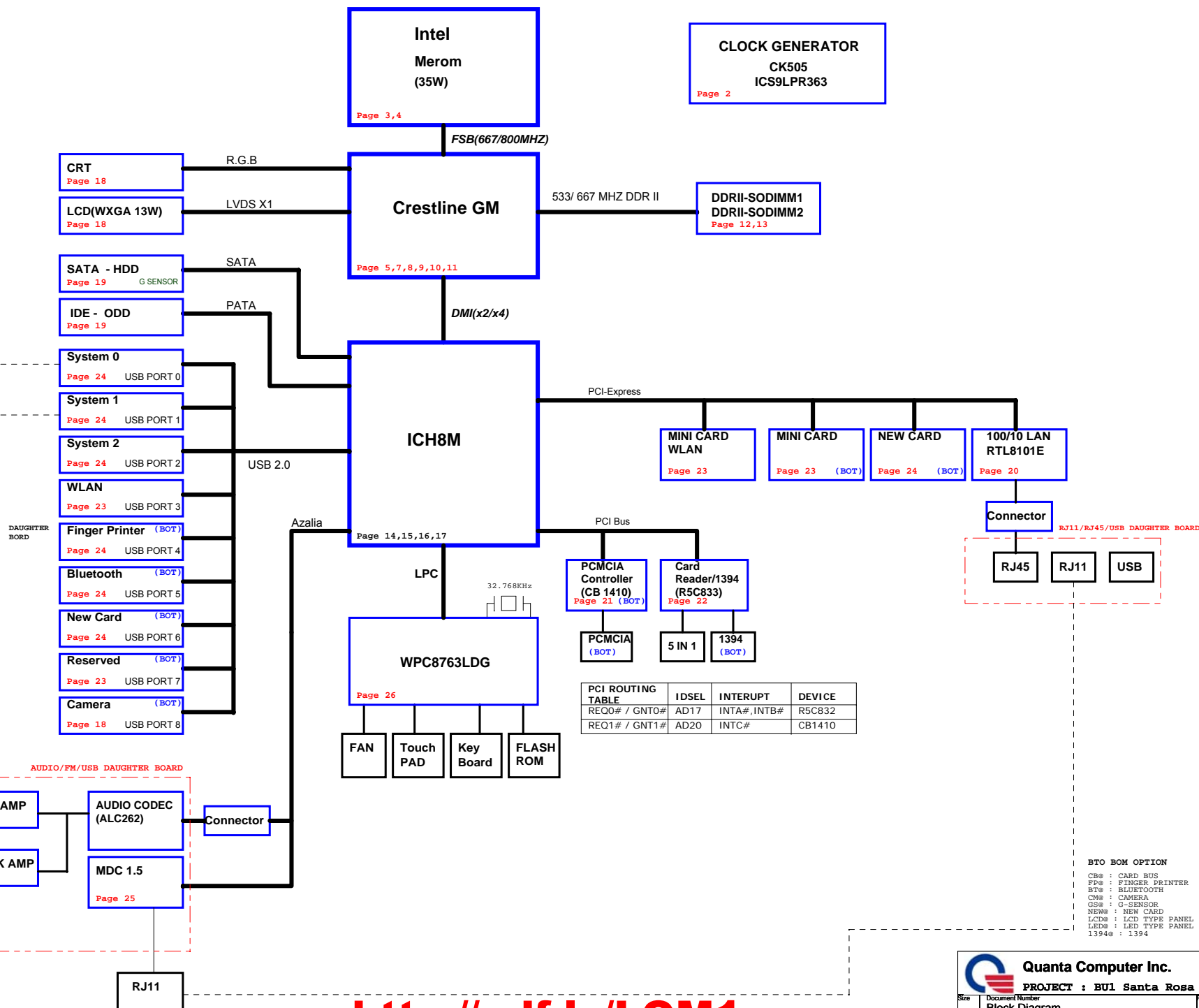
+1.05V

+1.25V

+1.8VSUS

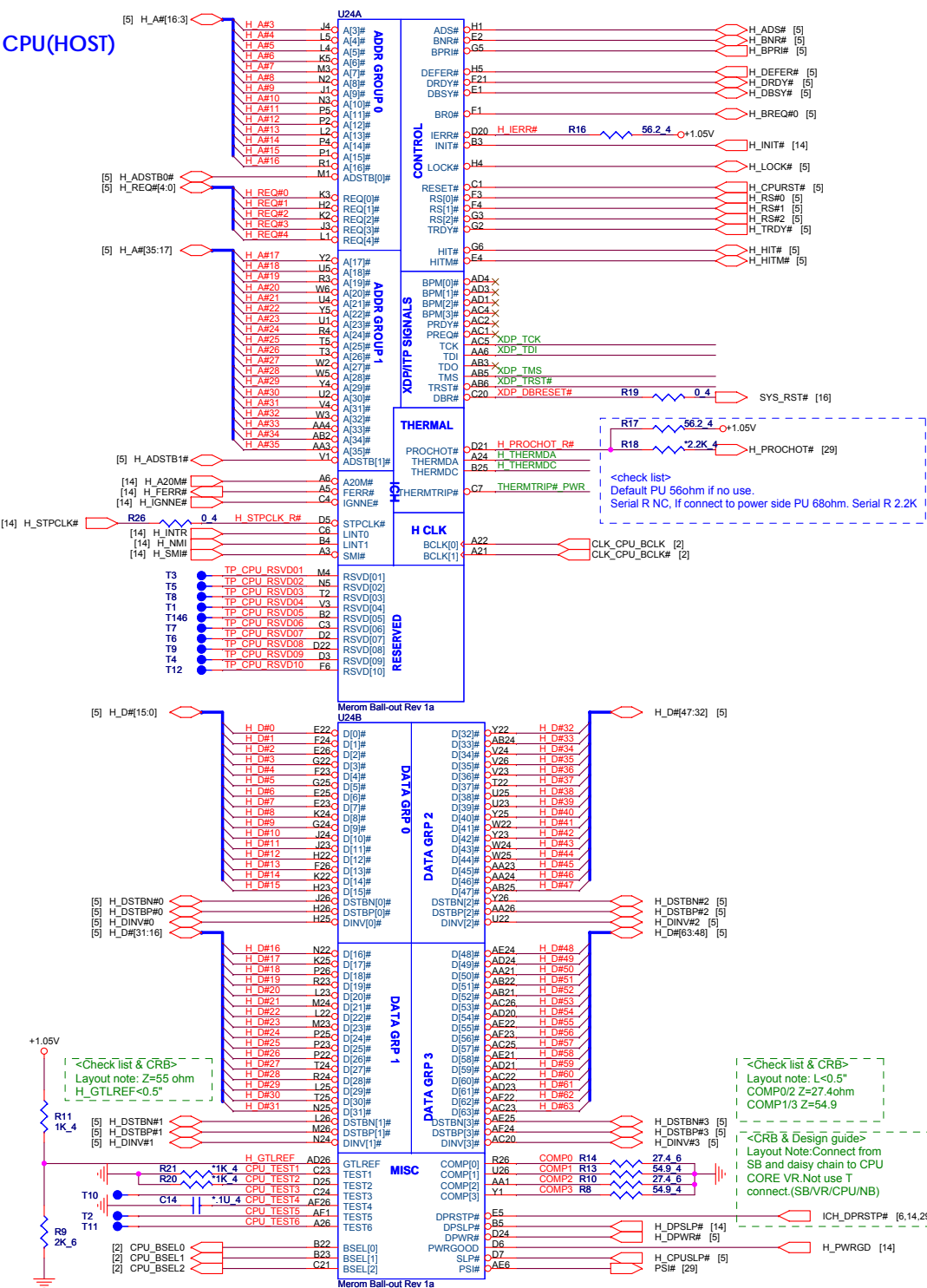
+3VPCU
+3V_S5
+3VSUS
+3V
+5VPCU
+5V_S5
+5V
SMDDR_VTERM
SMDDR_VREF

BU1 Block Diagram

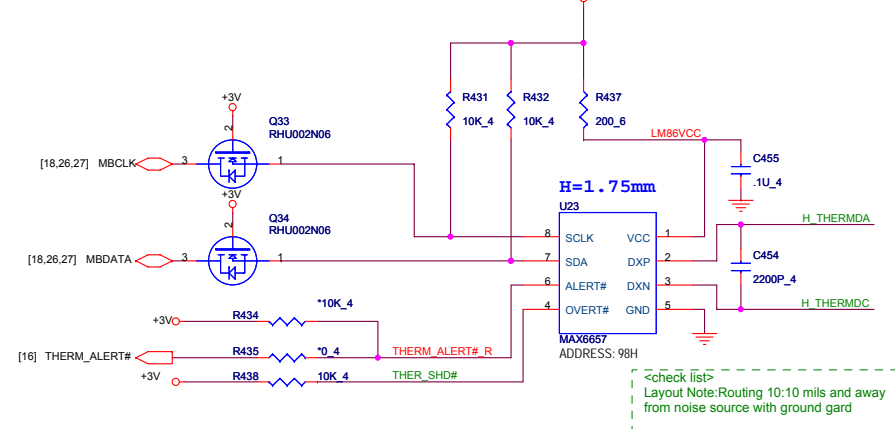


<http://adf.ly/LOM1>

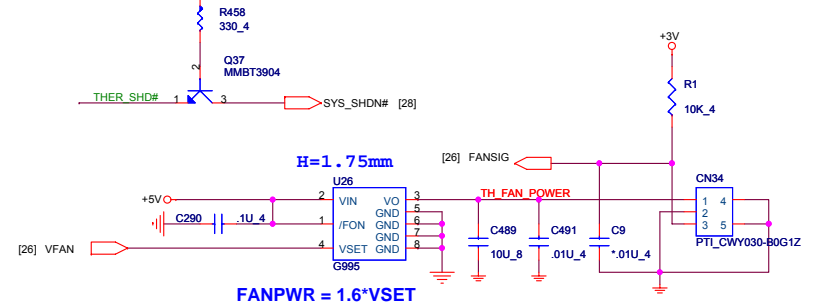
CPU(HOST)



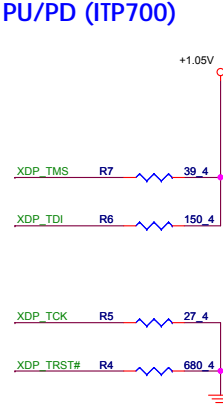
CPU Thermal monitor



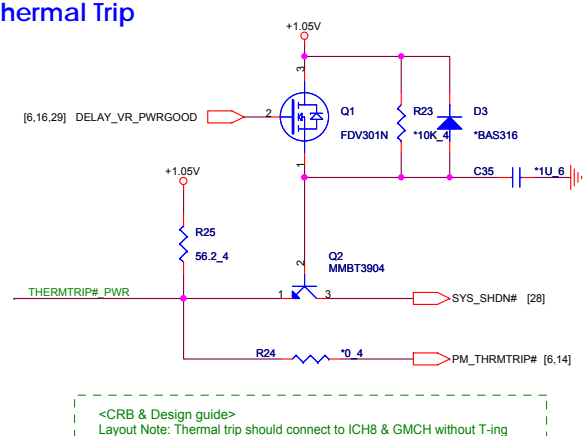
CPU FAN



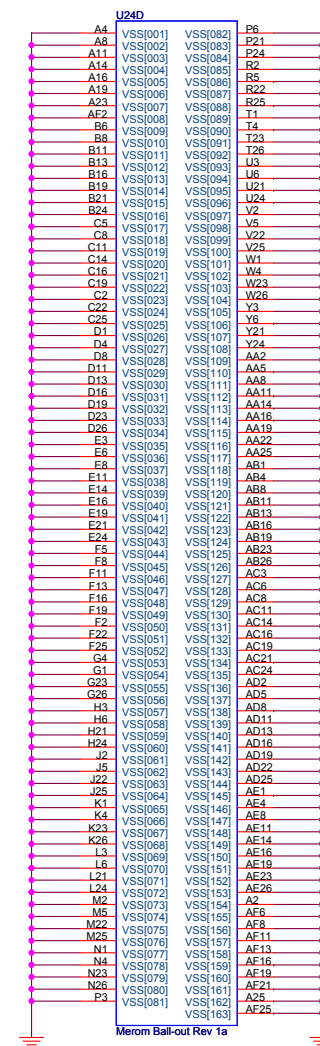
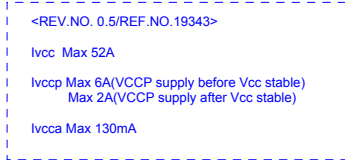
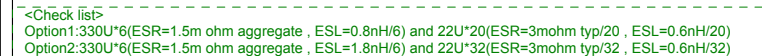
PU/PD (ITP700)

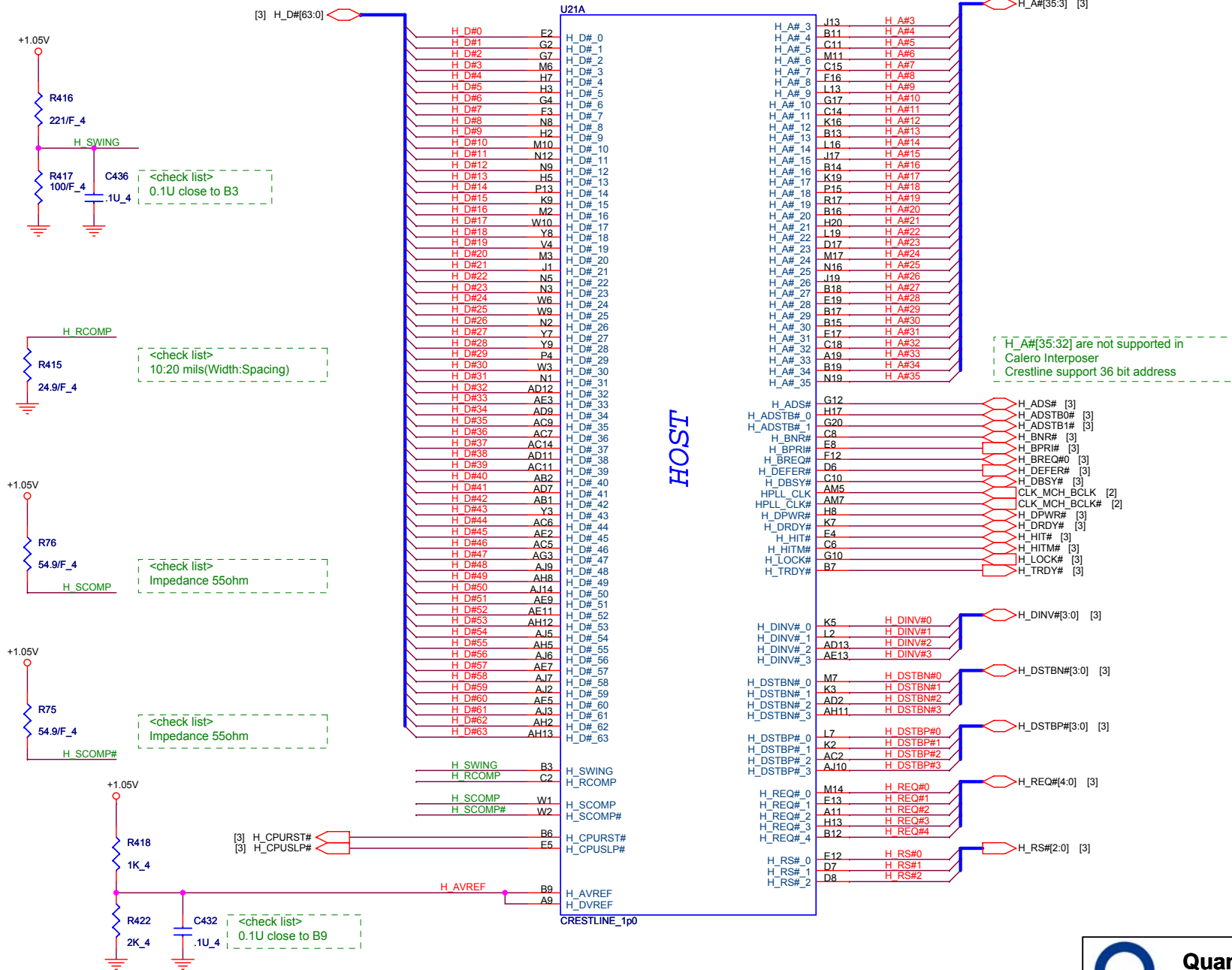


Thermal Trip



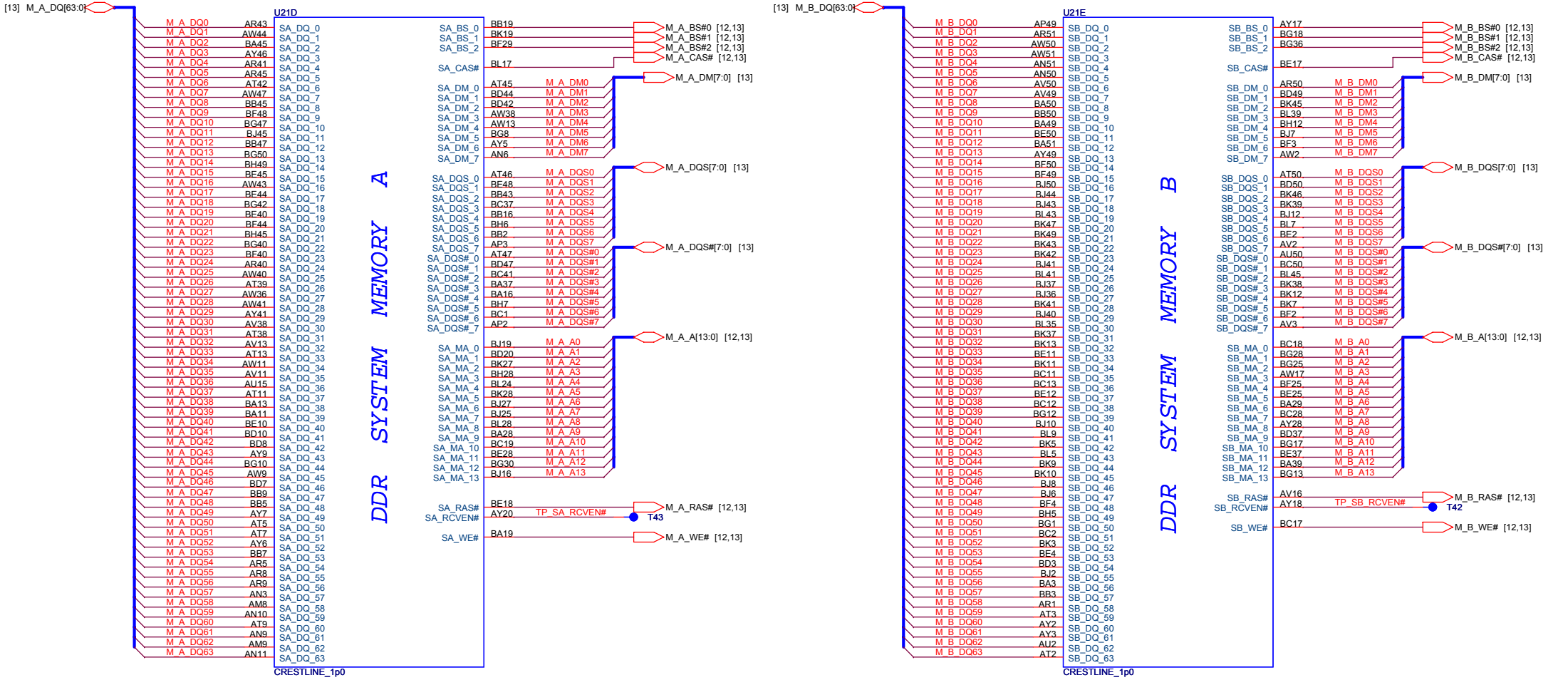
VCC_CORE








NB(Memory controller)



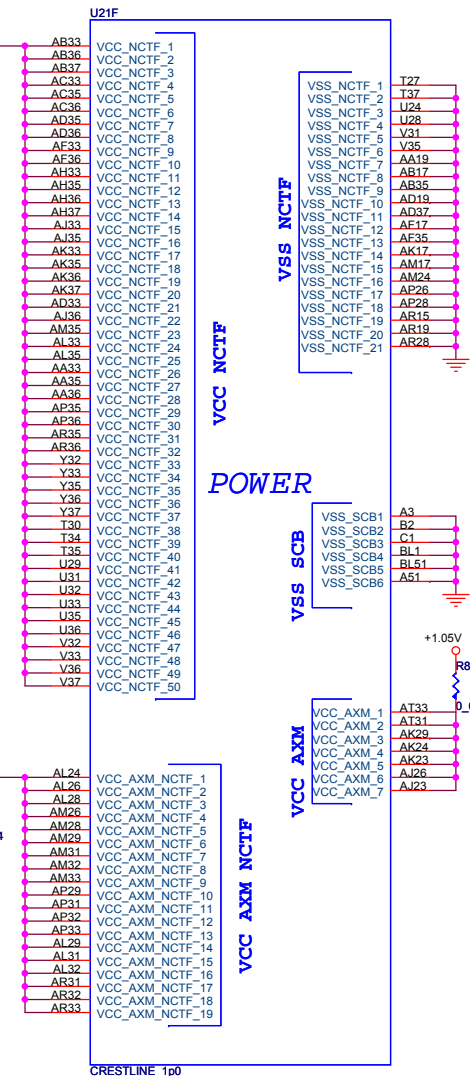
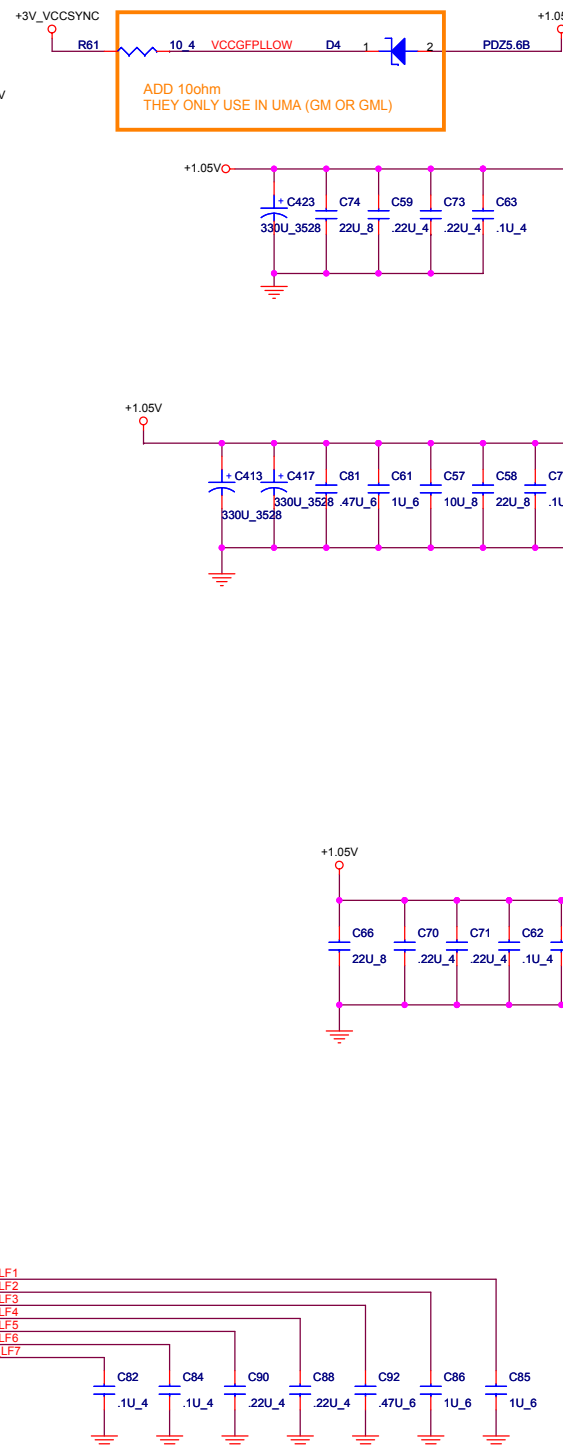
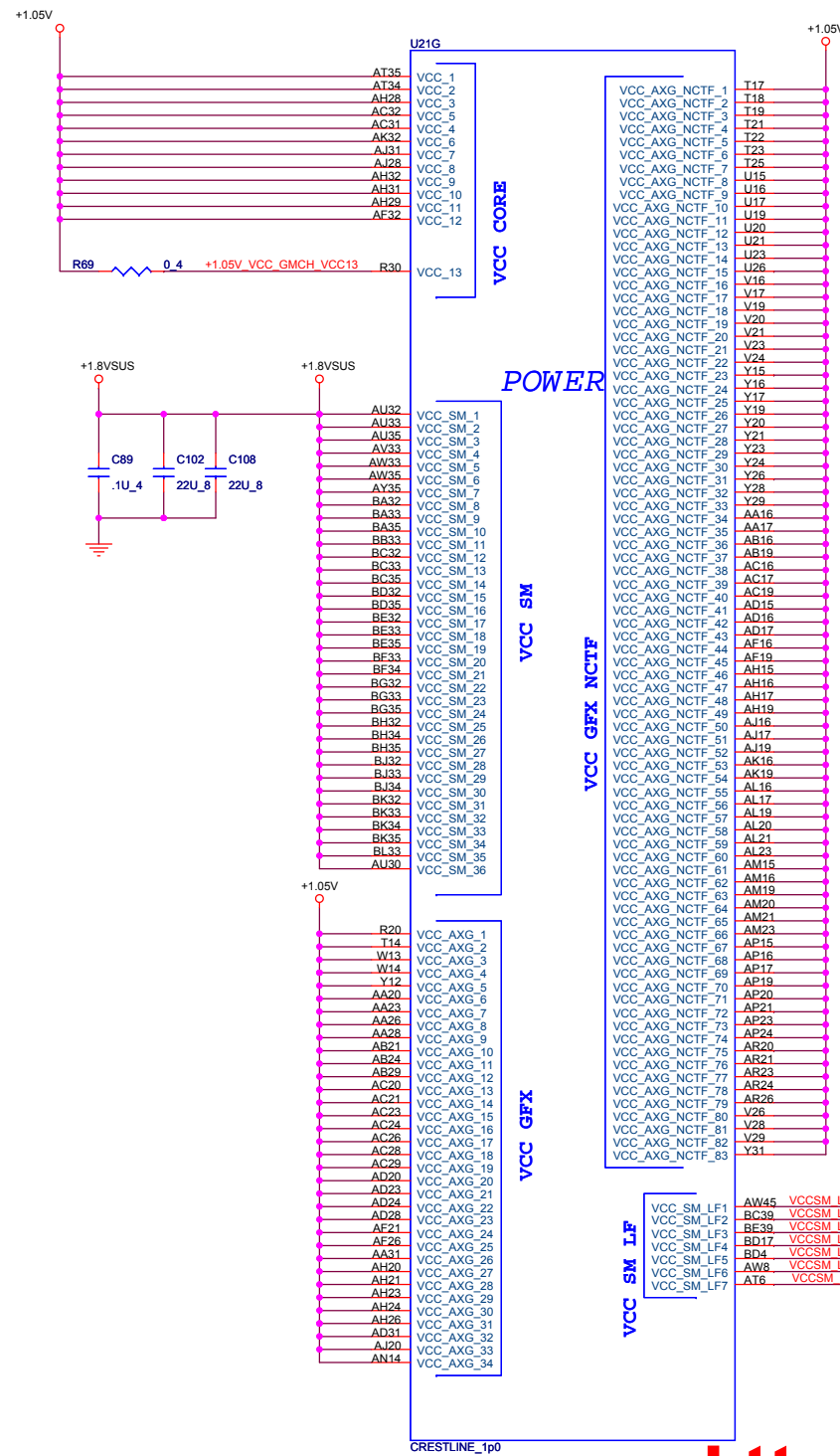


Quanta Computer Inc.
PROJECT : BU1 Santa Rosa

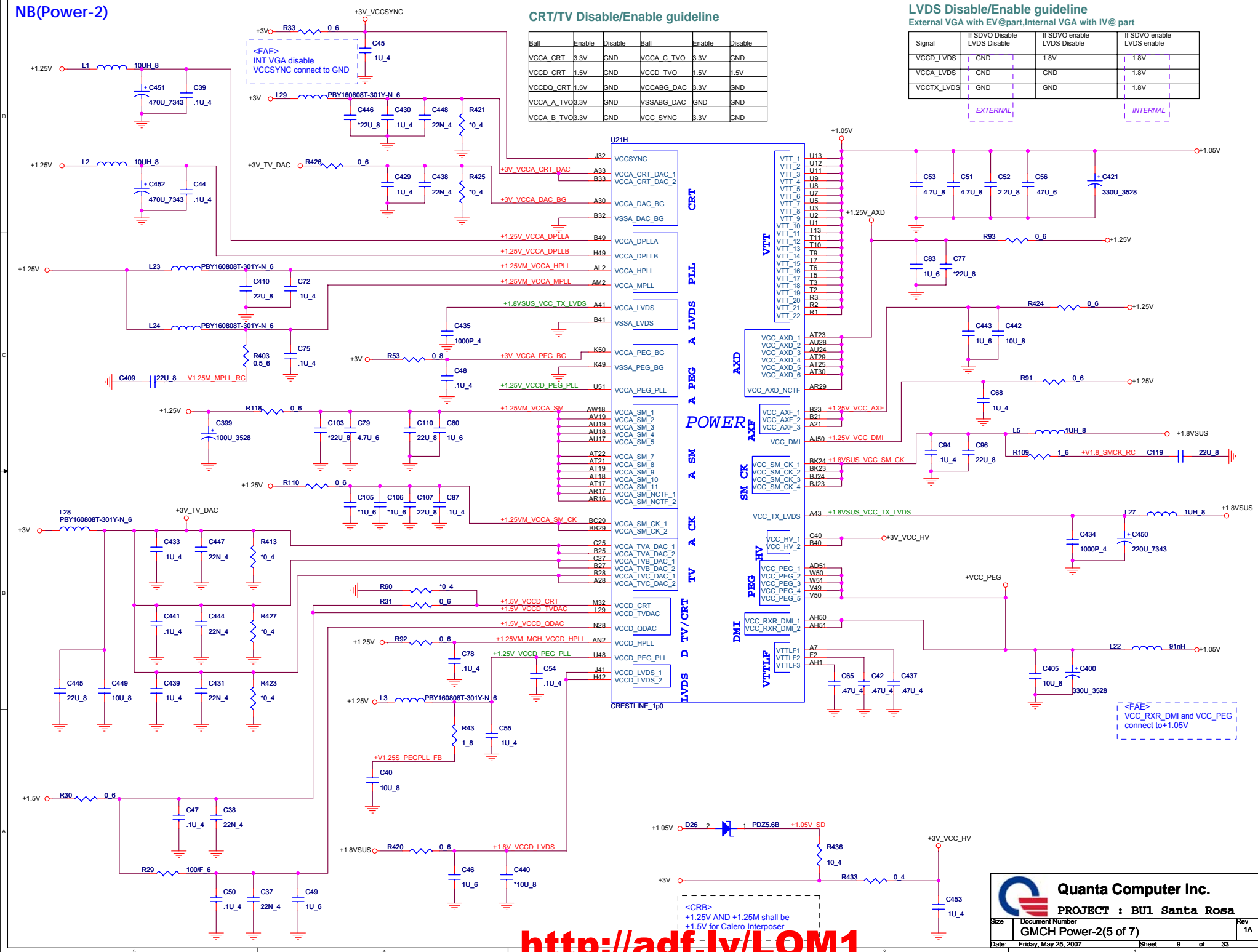
Size	Document Number	Rev
	MCH DDR(3 of 7)	1A
Date:	Friday, May 25, 2007	Sheet 7 of 33

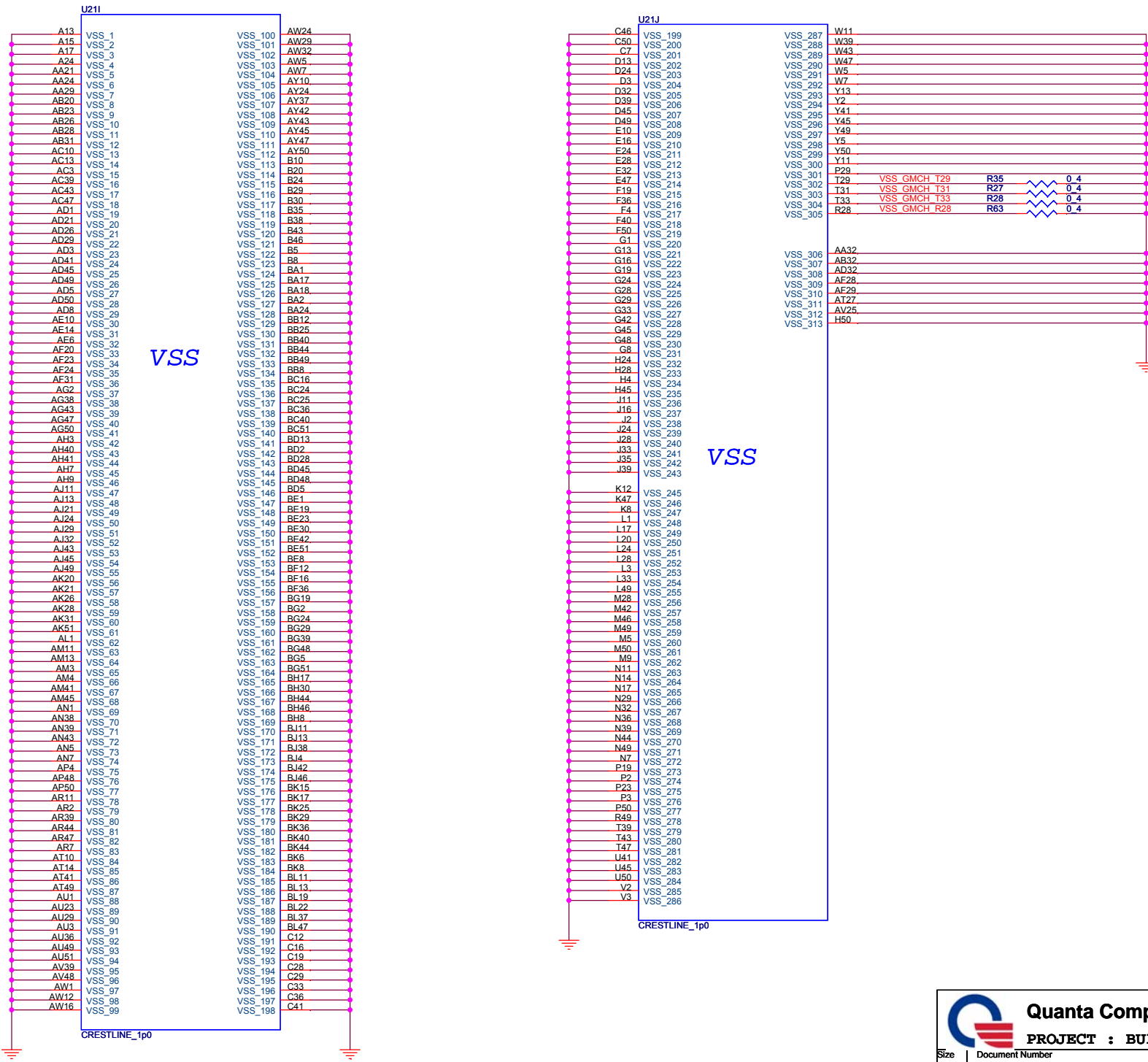
<http://adf.ly/LOM1>

NB(Power-1)



NB(Power-2)





Strap table

All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port

DMI X2 Select

MCH_CFG_5	Low = DMIX2 High = IDMIx4(Default)
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FSB Dynamic ODT

MCH_CFG_16	Low = ODT Disable High = ODT Enable(Default)
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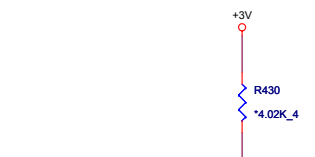
DMI Lane Reversal

MCH_CFG_19	Low = Normal operation(Default) High = Reverse Lane
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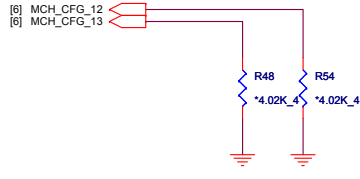
SDVO/PCIE Concurrent operation

MCH_CFG_20	Low = Only SDVO or PCIE X1 is operational(Default) High = SDVO andPCIE X1 are operating simultaneously via the PEG port
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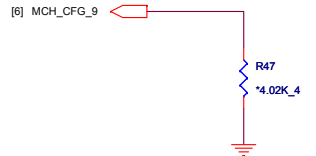
XOR /ALLz /Clock Un-gating

MCH_CFG_12	MCH_CFG_13	Configuration
0	0	Clock gating disable
0	1	XOR Mode Enable
1	0	ALL-z Mode Enable
1	1	Normal operation(Default)



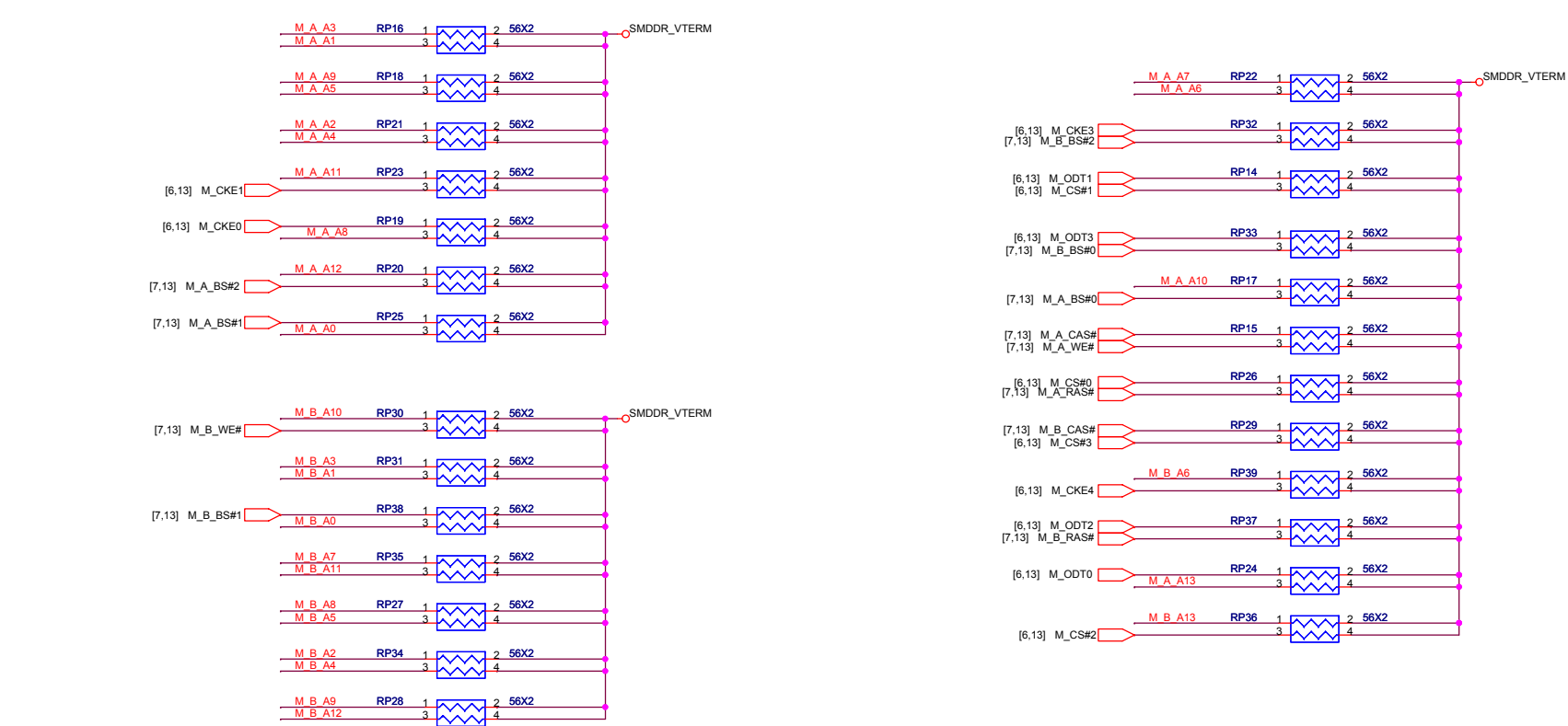
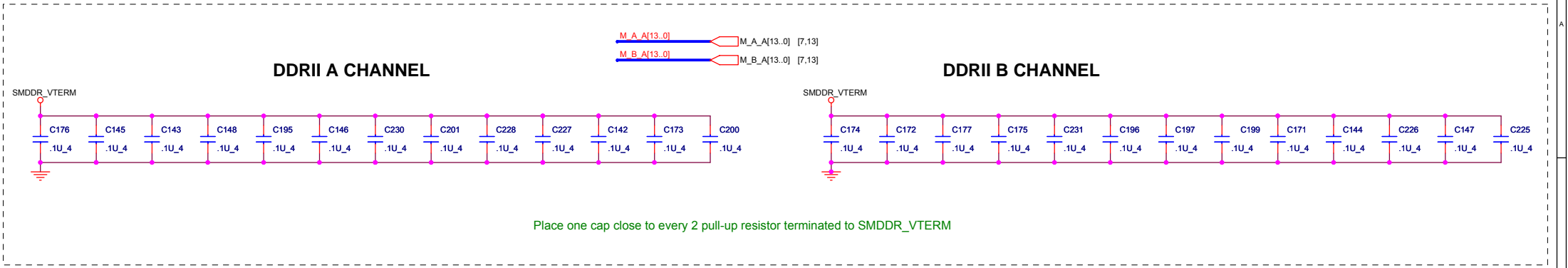
PCI Express Graphics

MCH_CFG_9	Low = Reverse Lane High = Normal operation(Default)
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SDVO Present

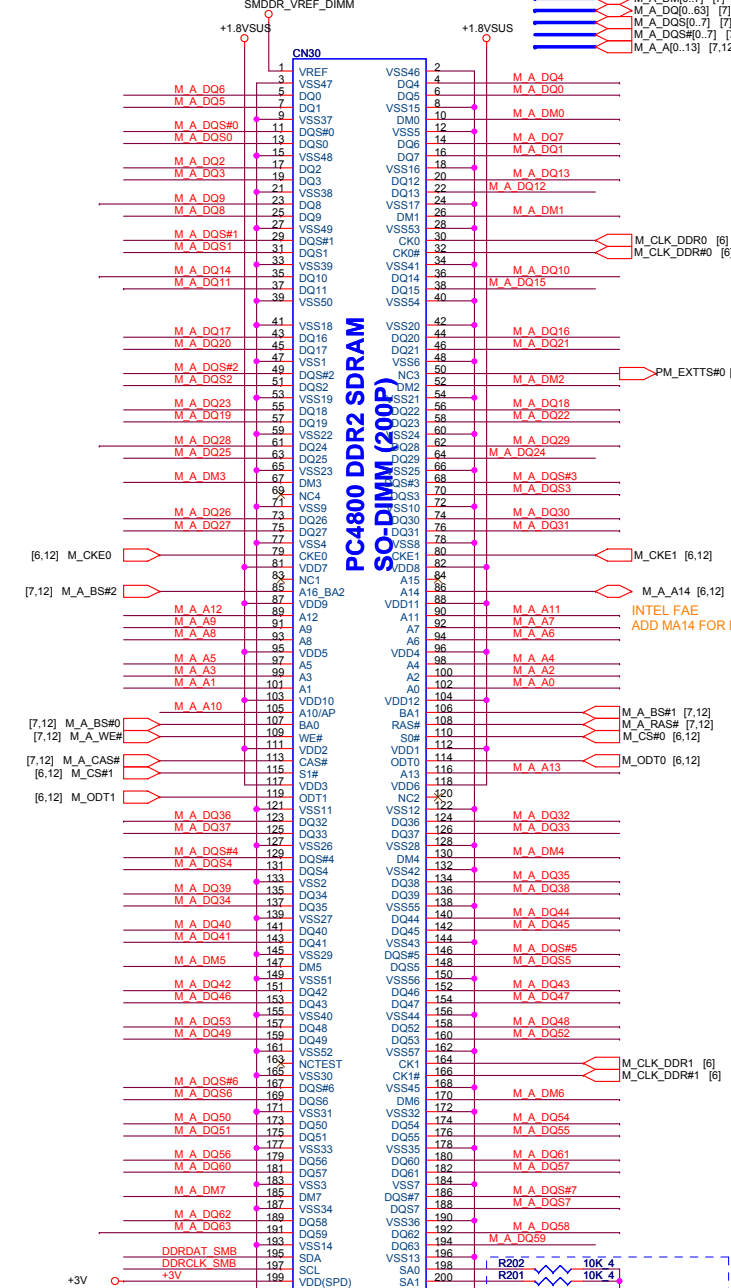
Strap define at External DVI control page



INTEL FAE
ADD MA14 FOR DUAL LAYERS RAM

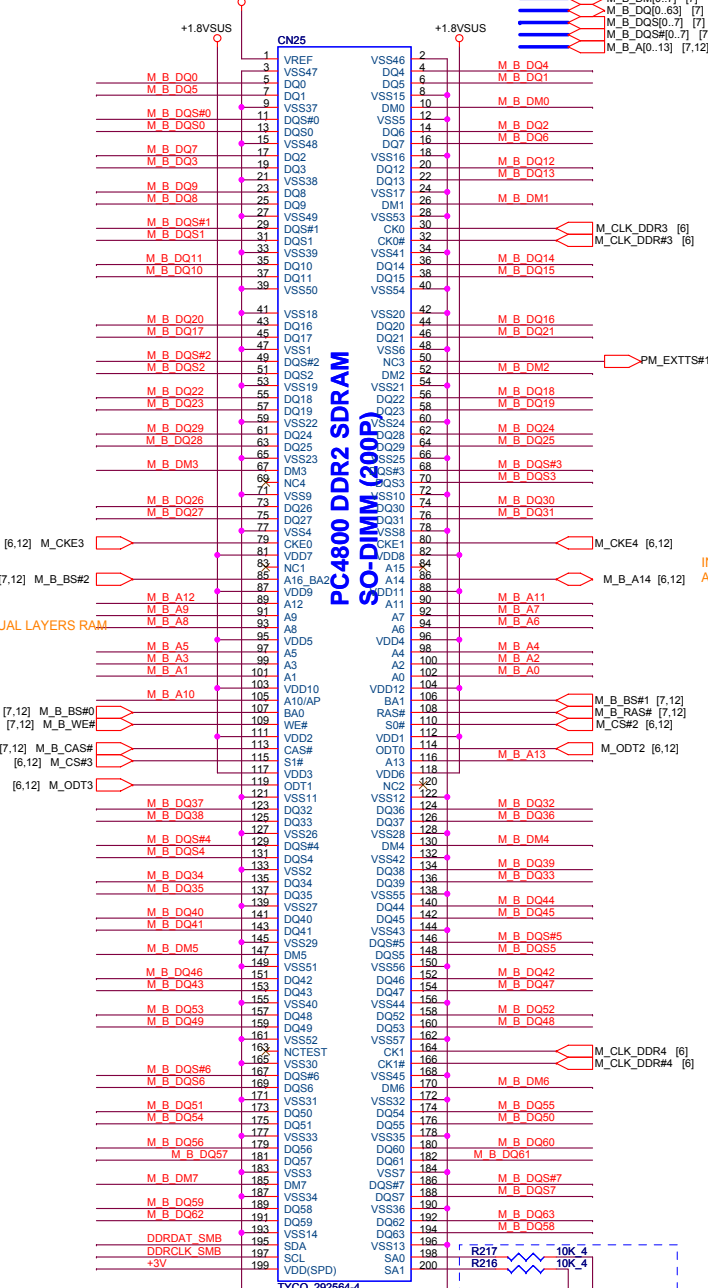
The diagram shows a signal line for MA14 with two pull-up resistors, R199 and R219, connected to a common SMDR_VTERM line. The resistors are labeled 56.4 and 56.4 respectively.

DDR2 Dual channel A/B CONN



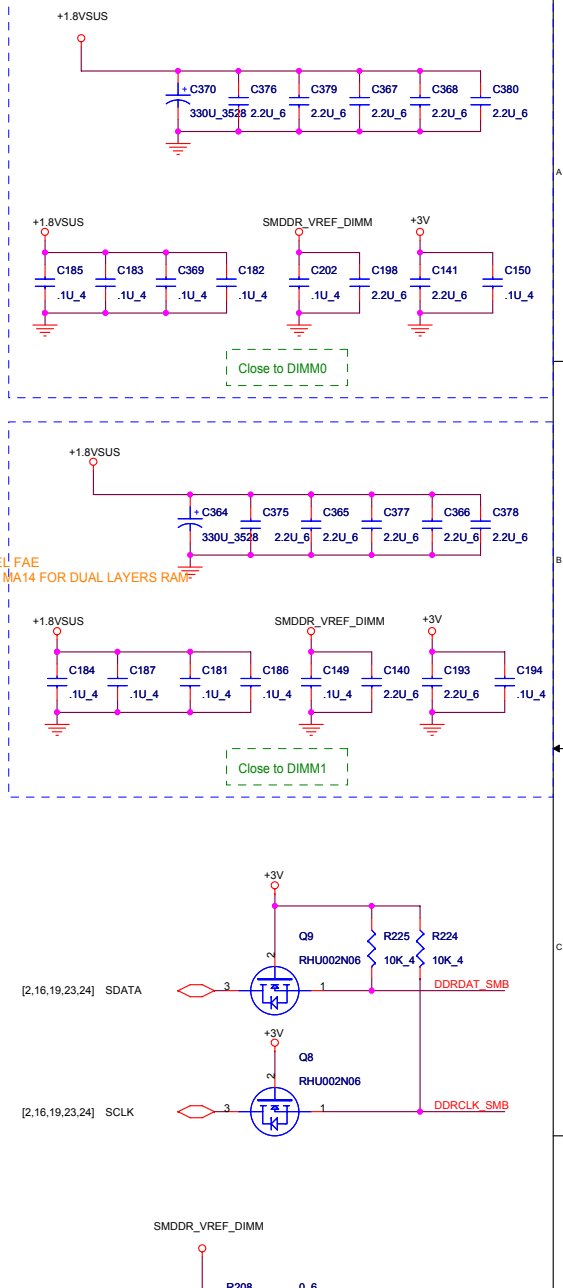
SLOT A
H: 5.6mm

CLOCK 0,1
CKE 0,1



SLOT B
H: 10.1mm

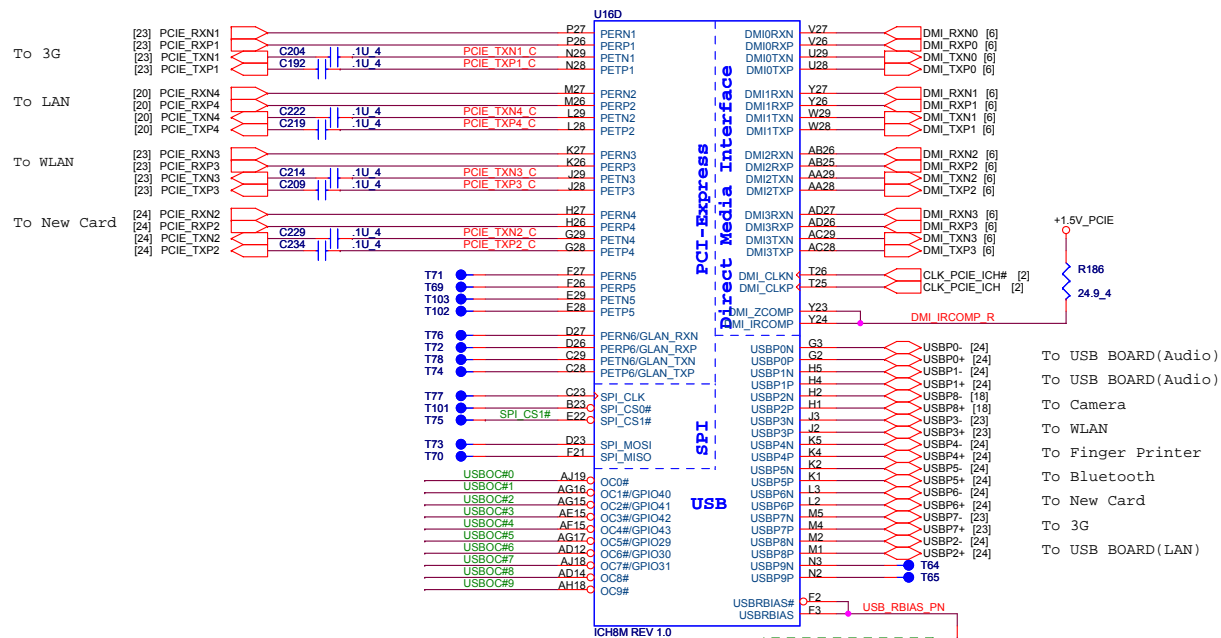
CLOCK 3,4
CKE 2,3



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PROJECT : BU1 Santa Rosa
DDR SO-DIMM(200P)
Date: Friday, May 25, 2007 Sheet 13 of 33

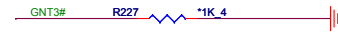
<http://adf.ly/LOM1>

SB-PCIE/USB/DMI



A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default
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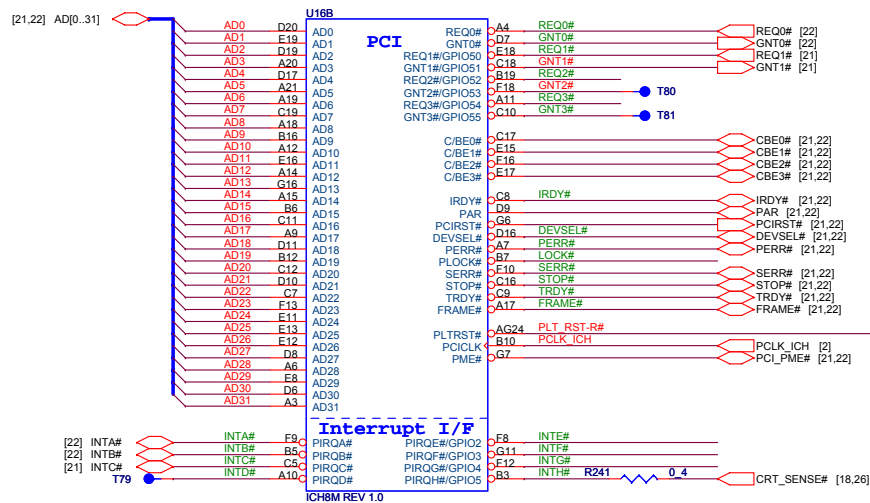


ICH8 Boot BIOS select

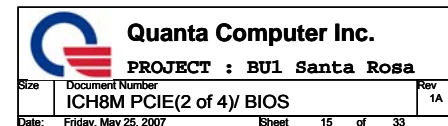
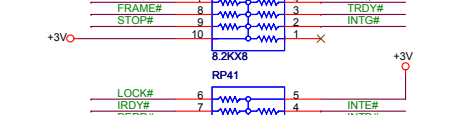
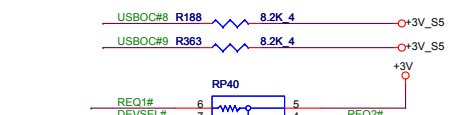
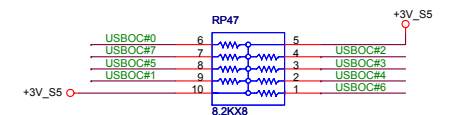
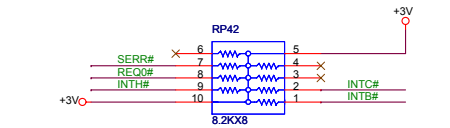
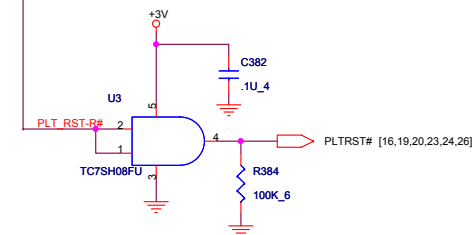
PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC



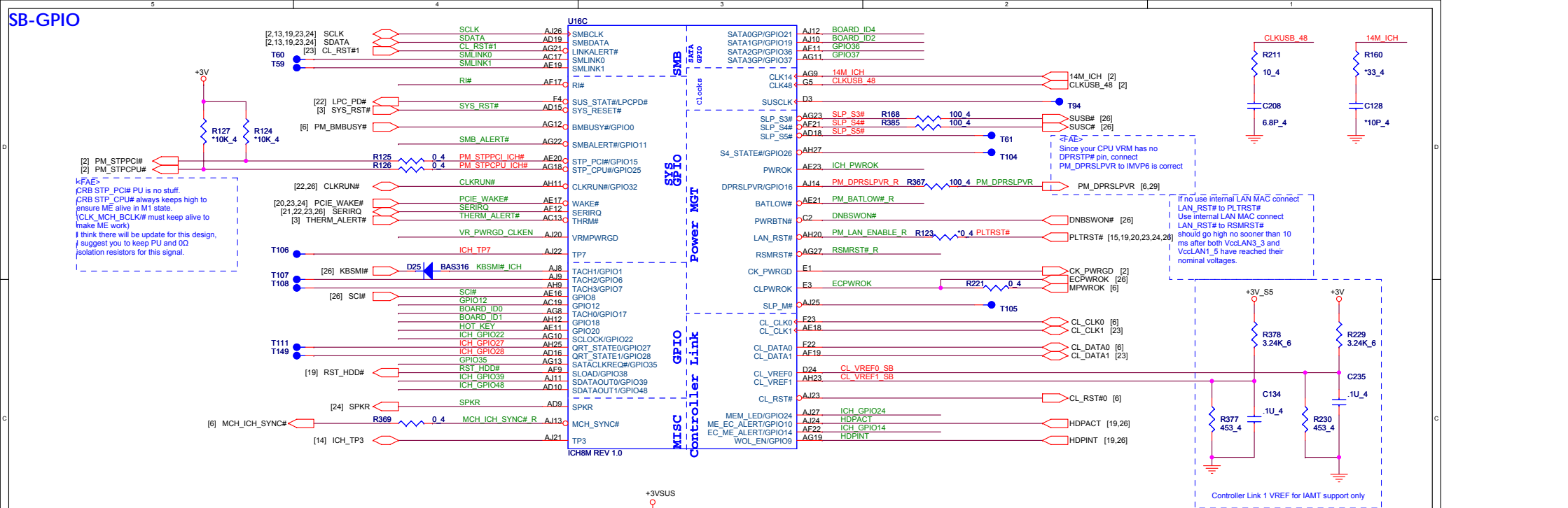
SB-PCI



PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#,INTB#	R5C833
REQ1# / GNT1#	AD20	INTC#	CB1410



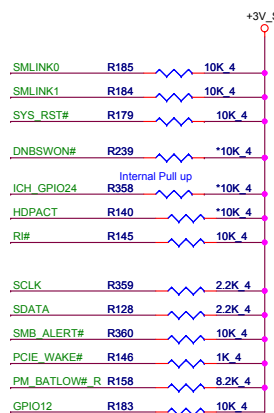
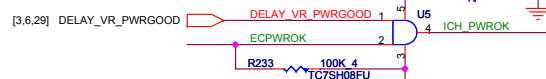
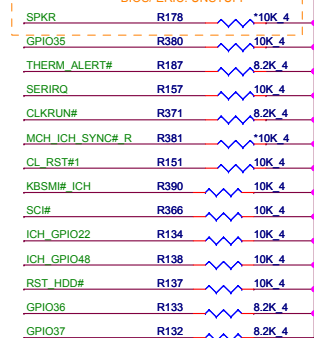
SB-GPIO



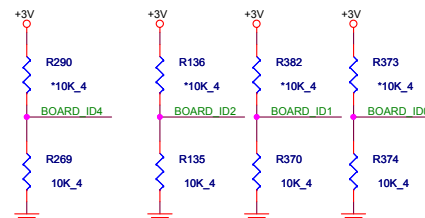
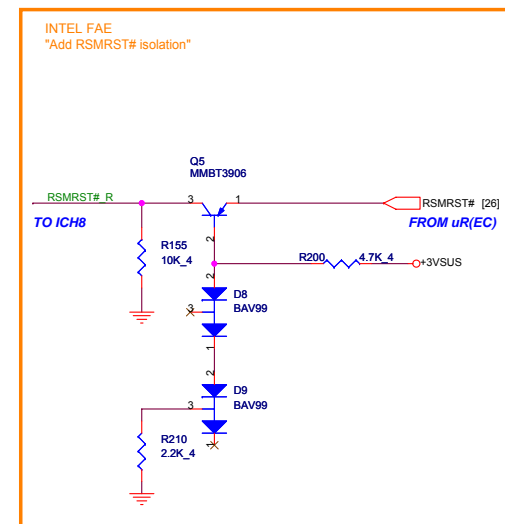
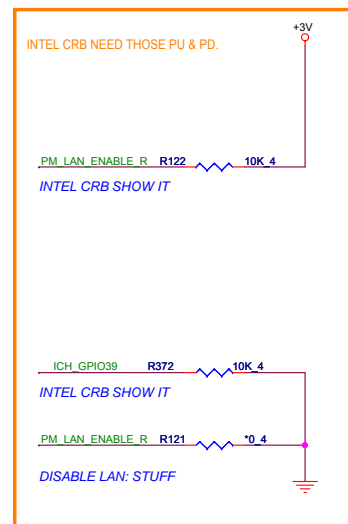
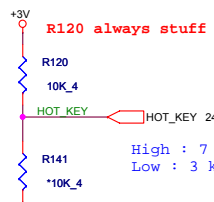
No Reboot strap

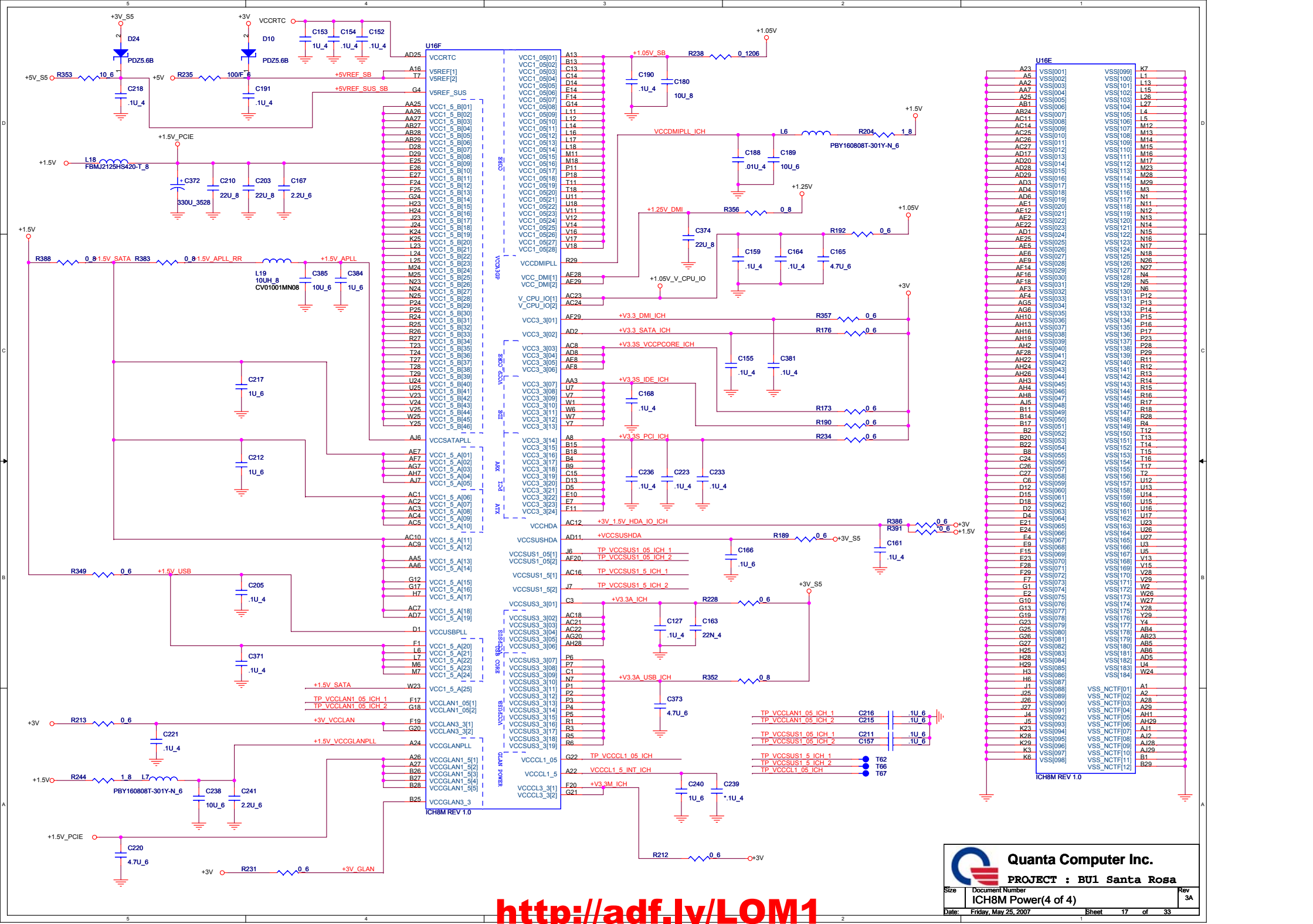
SPKR	Low = Default High = No Reboot
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BIOS/ ERIC: UNSTUFF

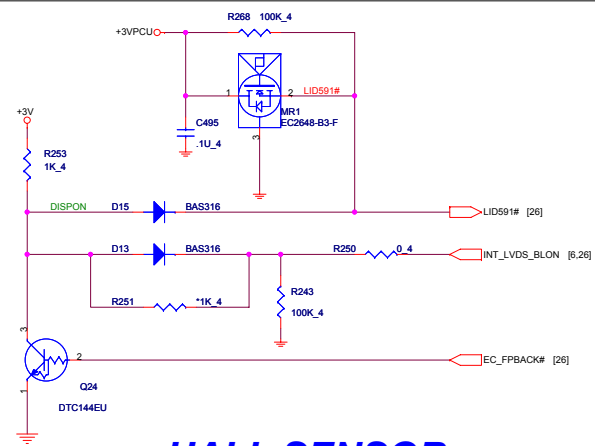
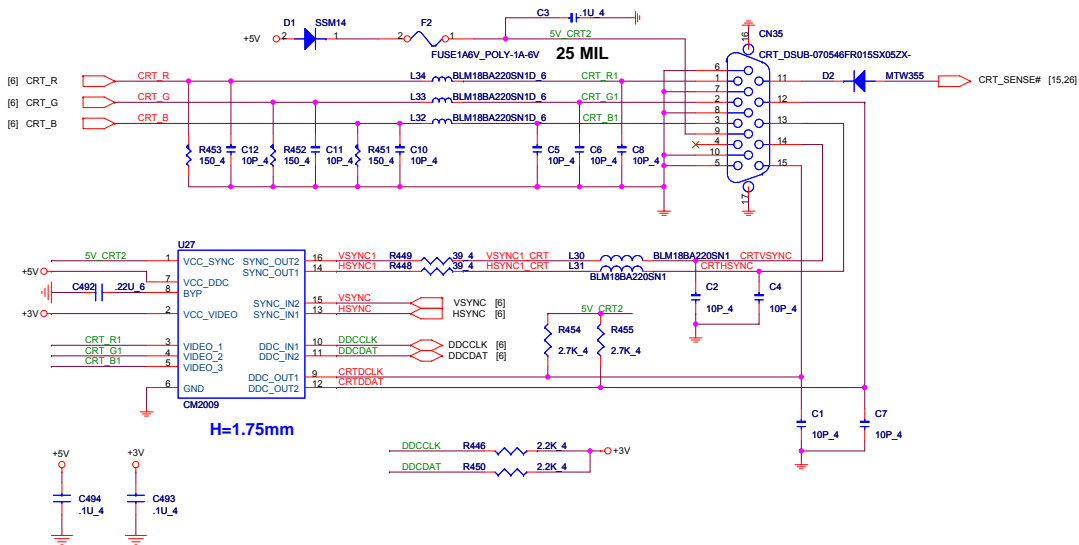


Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel				H L	
W/ G-SENSOR W/O G-SENSOR			H L		
7 HOT_KEY 3 HOT_KEY		H L			
W/ ROBSON W/O ROBSON	H L				



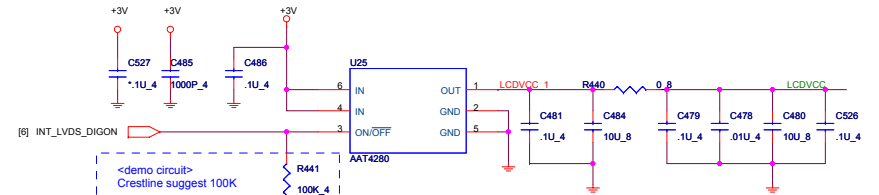
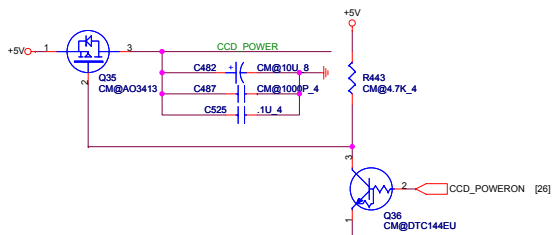


CRT PORT

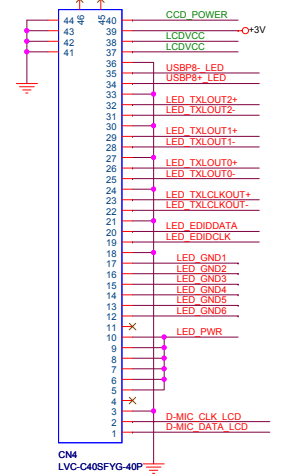
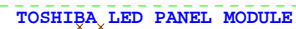
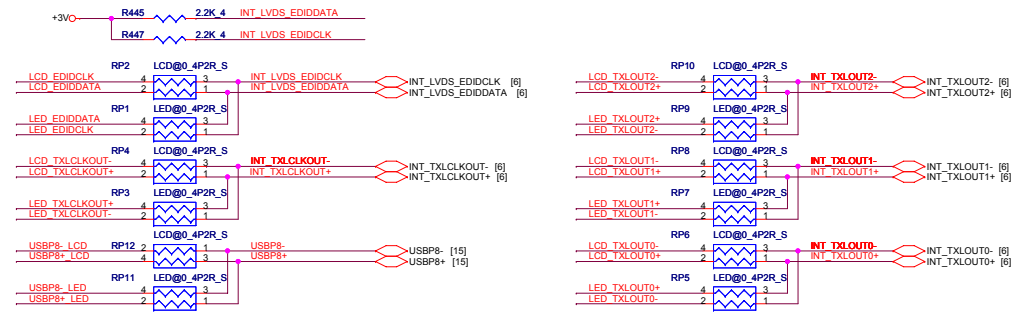


HALL SENSOR

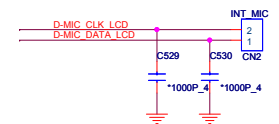
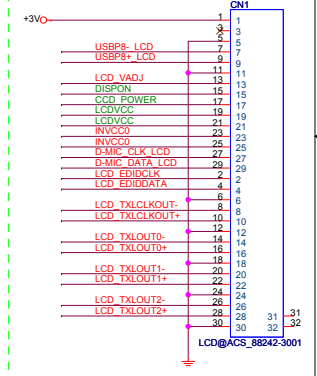
CAMERA MODULE

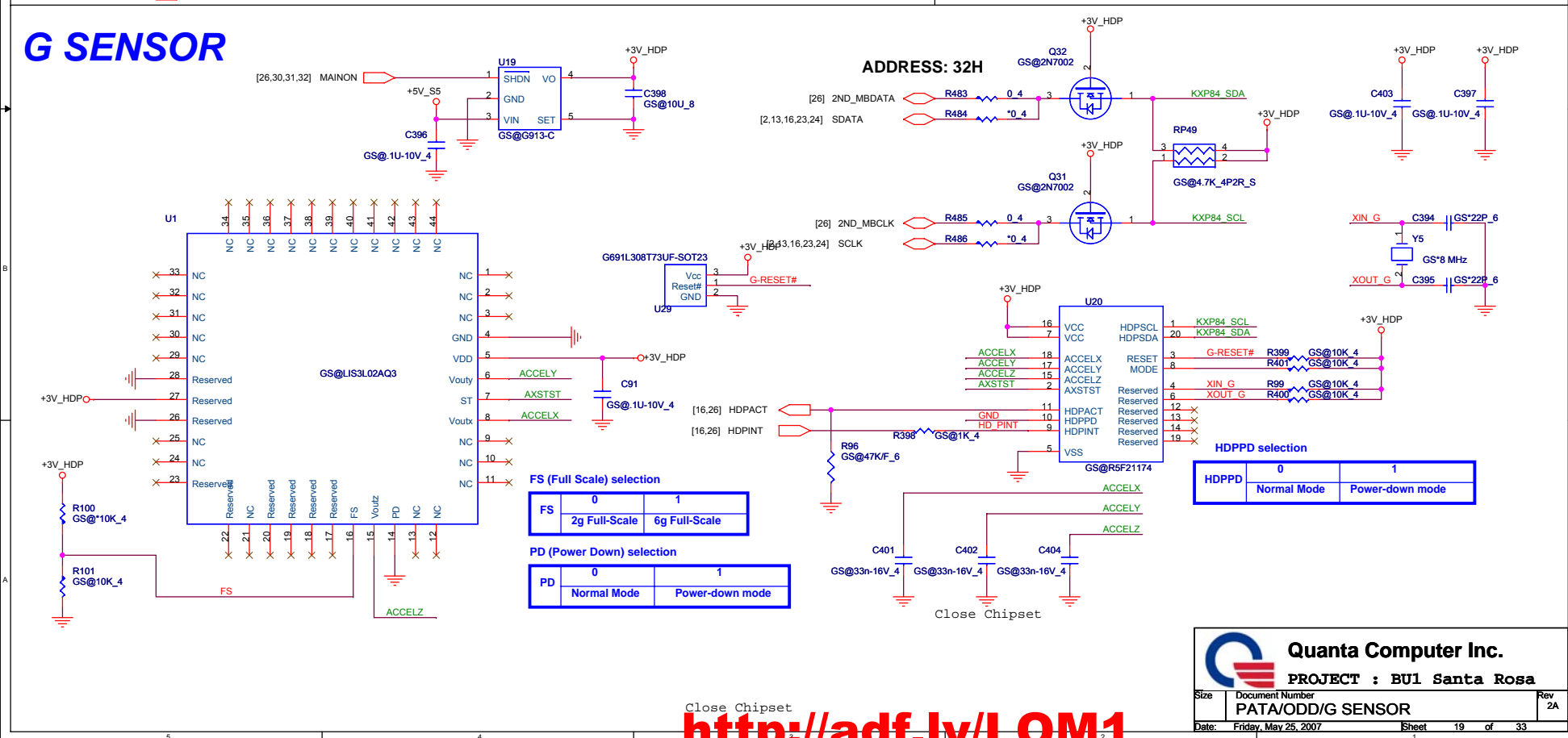
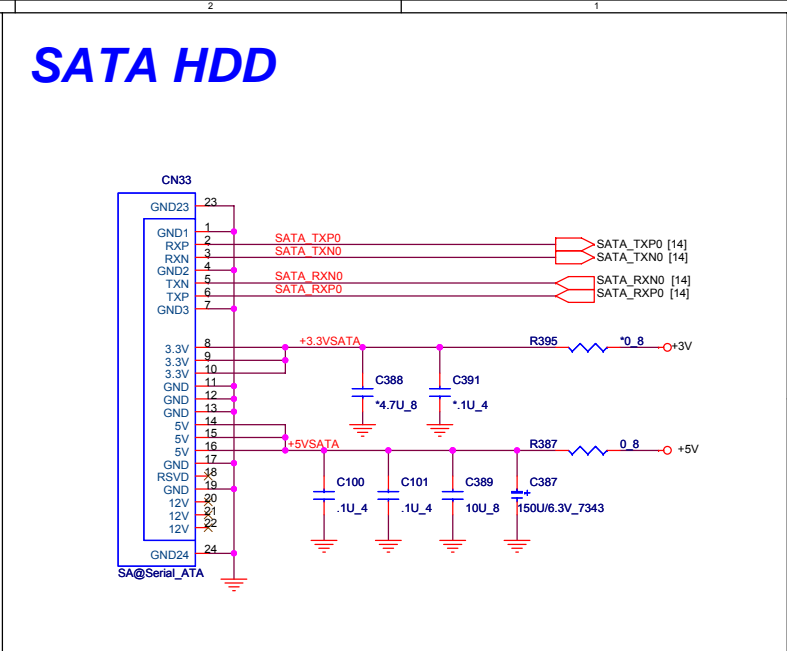
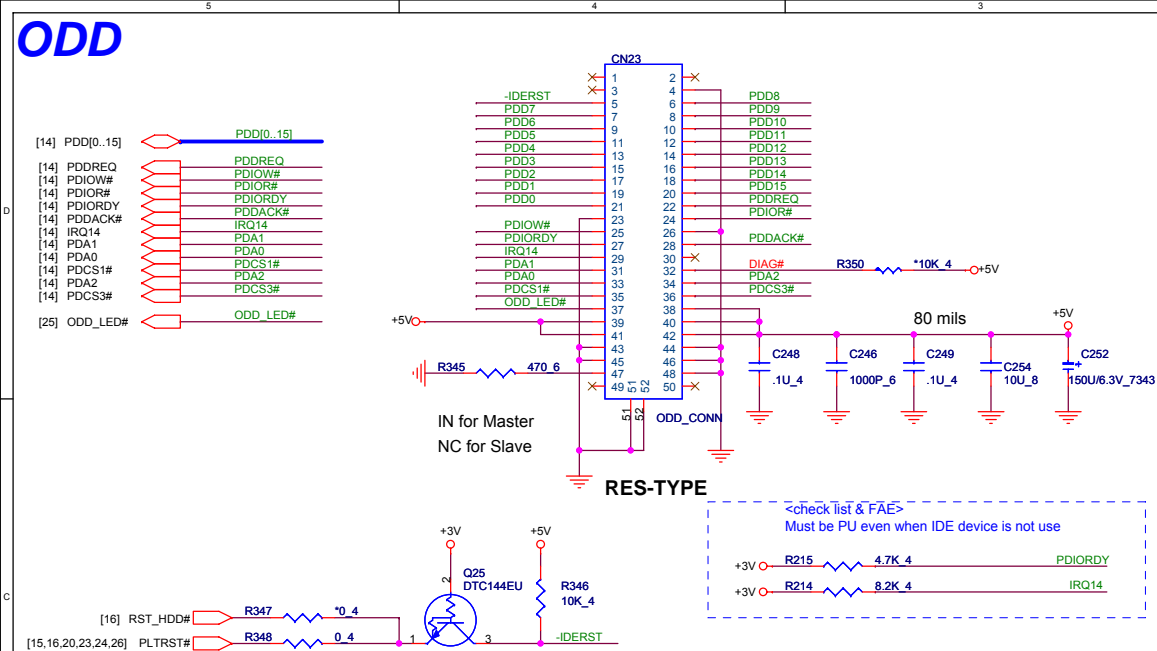


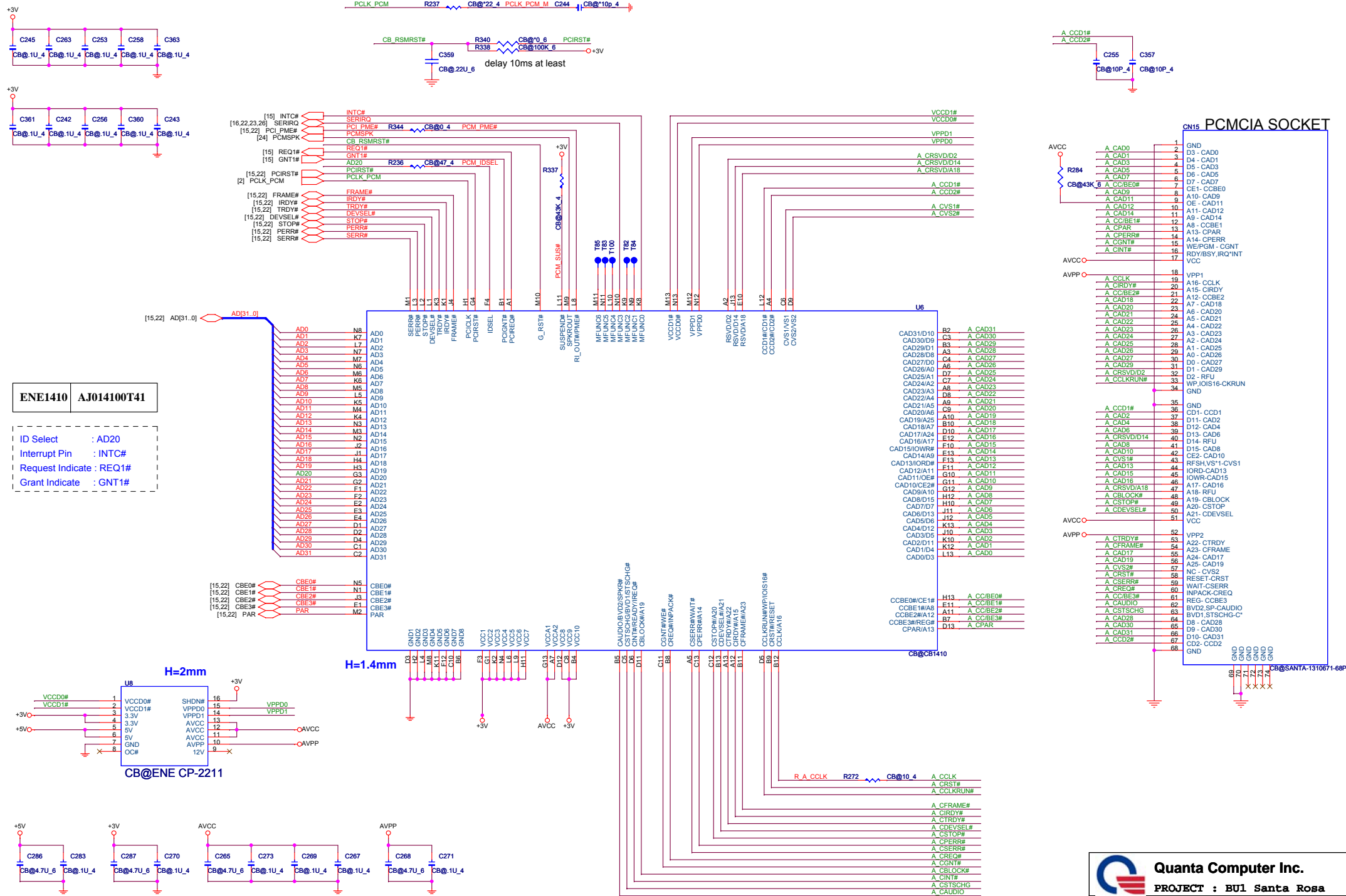
LCD/LED TYPE CONNECTOR



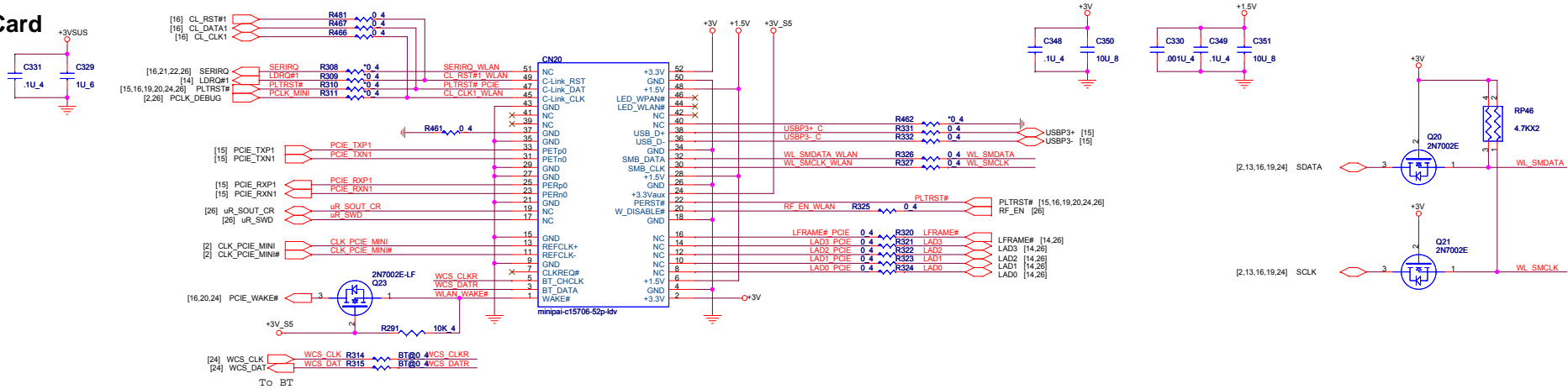
LCD PANEL MODULE



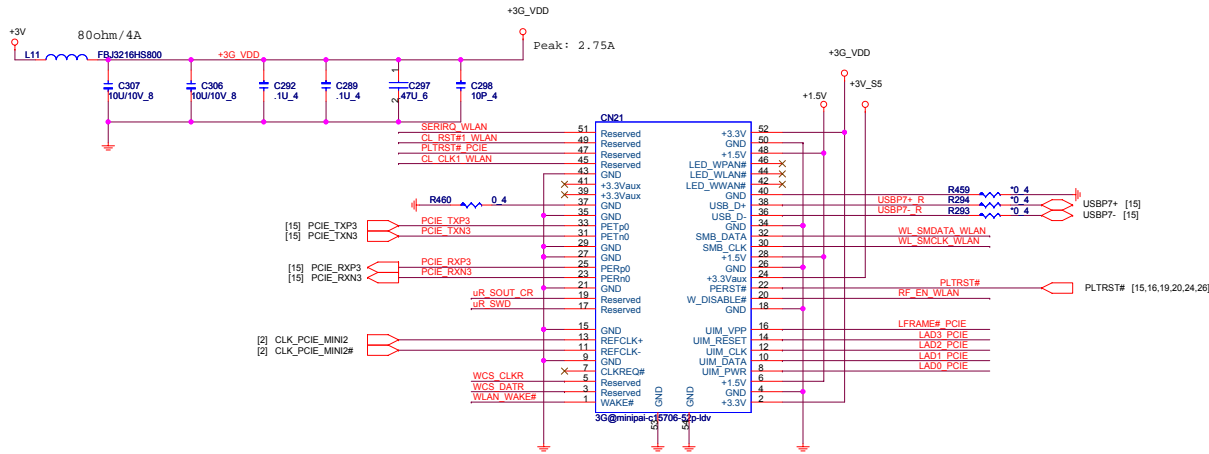




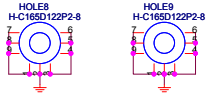
Mini PCI-E Card WLAN



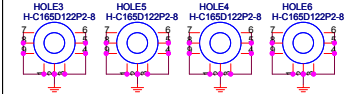
MINI-Card



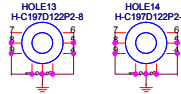
NB SINK



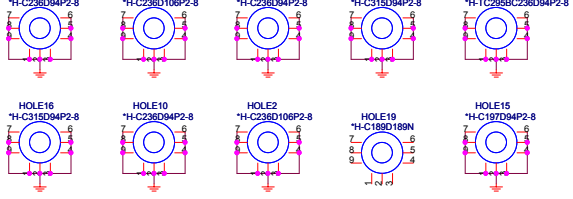
CPU SINK



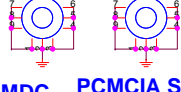
MINI CARD SINK



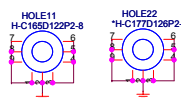
MB SINK



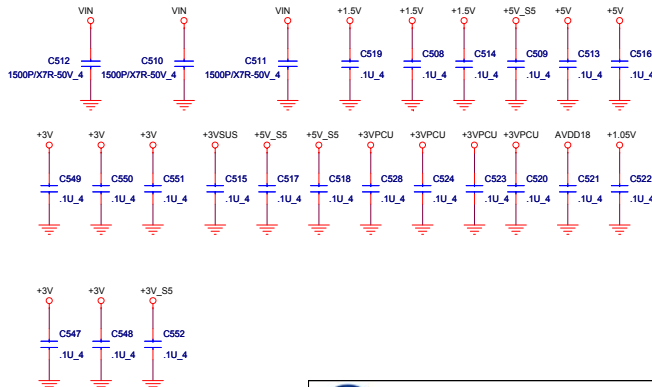
PCMCIA SINK

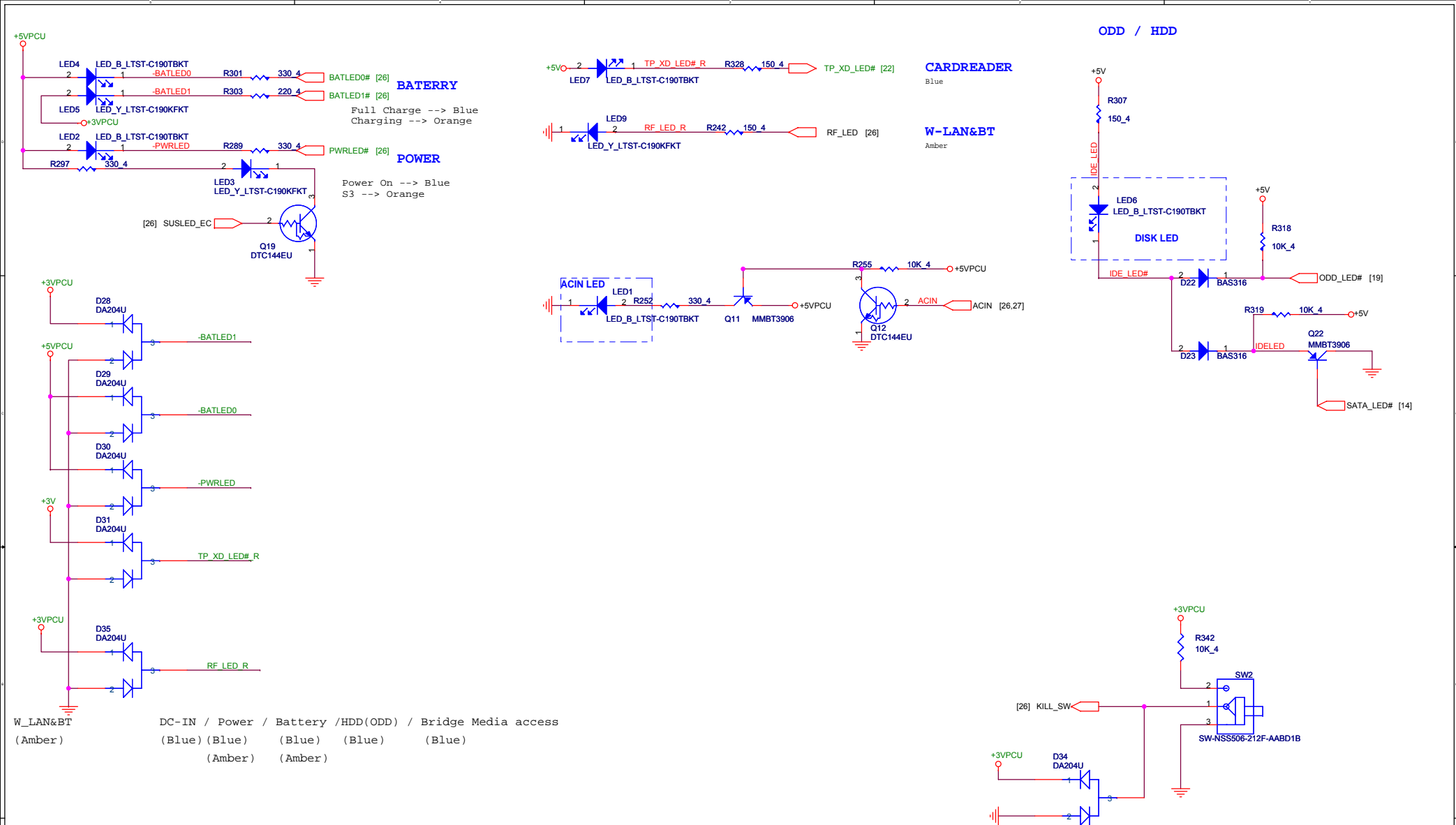


MDC PCMCIA SINK

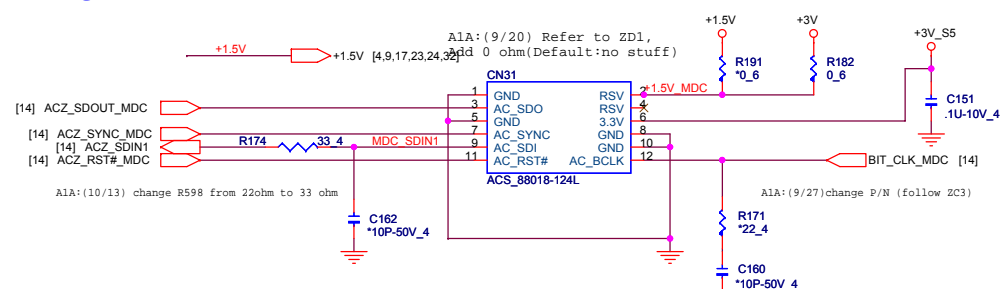


FOR EMI





MDC



Model	REV	DATE	CHANGE LIST	NOTE
BU1	00	20061218	FIRST RELEASED : 20061218	
	01	20061225	Page02: Change CLK GEN. low power outs from +1.05V to +1.25V.Because VDD_IO will drop out when high loading	Circuit modify
			Page02: REV_01 Remove CLK_MCH_OE#_R had pull up resistor,because had be pull up at NB side	Circuit modify
			Page03: Del R382,R383,Q60,D39	Circuit modify
			Page04: Del R176 for FBS signals batter return path under +1.05V plane	Circuit modify
			Page08: Change Crestline VCC_AXM to 1.25V, reference to SR ww48 MoW. reserved 0 ohm resister	Circuit modify
			Page16: Add D43 to avoid leakage from EC to SB,Del R242	Circuit modify
			Page18: REV_01 Reserved LCD/LED type panel module and Digital/analogy MIC	Circuit modify
			Page19: Modify G-Sensor circuit	Circuit modify
			Page22: Reserved LPC_PD# control signal from SB to R5C833	Circuit modify
			Page23: Increase HOLE	Circuit modify
			Page24: Add 0.1u CAP. C810 from +5VPCU to GND	Circuit modify
			Page25: Modify IDE LED circuit	Circuit modify
			Page26: Reserved R756,R766 for EC control G-Sensor	Circuit modify
			Page27: Add 3 cell Battery always setting circuit	Circuit modify
			Page28: Add +3V_S5 discharge circuit	Circuit modify
			Page30: Reserved PD resistor to avoid leakage voltage	Circuit modify
			Page32: Reserve +3V discharge circuit	Circuit modify
	1A	20061227	A TEST (PCB REV_1A) RELEASED : 20061227	
	2A	20070201	Page03: Modify thermal protect circuit and FAN control	Circuit modify
			Page14: Modify RTC charge current / SB strip setting / Reserved PU resistor on SATALED# signal / Change XTAL capacitor value	BOM/Circuit modify
			Page16: Reserver Pull down resistor on HDPINT signal / Reserved C-Link to WLAN / Delete FM function / Add Board ID	Circuit modify
			Page18: Change panel backlight signal pull up resistor / Change camera power source / Add LED type panel circuit / Add fuse on CRT power	BOM/Circuit modify
			/ Reserved EMI choke on USB signals and add EMI solution / Add RC circuit on LED panel driver IC	Circuit modify
			Page19: Modify LDO power source / Add Microprocessor reset IC / Reserved G-sensor SMBUS to SB chipset	Circuit modify
			Page22: Reserved Cardreader external EEPROM	Circuit modify
			Page23: Separate RF enable/disable pin from WLAN and 3G card / Add EMI solution and Reserved C-Link circuit / Delete 3G card function	Circuit modify
			/ Add HOLE for card Bus connector	Circuit modify
			Page24: Increase CN7 pin for control illumination logo and enable/disable USB port power / Add capacitor on keyboard signals for EMI	Circuit modify
			/ Change LAN/B cable connector / Delete FM function	Circuit modify
			Page25: Modify battery LED and RF SW power source / Delete 3G card LED	Circuit modify
			Page26: Modify EC control circuit / Add EMI solution / Change XTAL capacitor value	BOM/Circuit modify
			Page27: Change fuse rating and switch MOS	Circuit modify
			Page29: Add EMI solution	Circuit modify
			Page30: Add EMI solution	Circuit modify
			Page31: Add EMI solution	Circuit modify
			Page32: Add EMI solution	Circuit modify
	3A	20070326	Page03: Add CAP to GND for FAN controller IC U12 power pin decoupling	Circuit modify
			Page13: Change DDR socket height	Circuit modify
			Page18: Exchange Dioid and Fuse placement	Circuit modify
			Page20: Add control LAN power circuit to enable/disable LAN	Circuit modify
			Page22: Change 1394 connector type and delete card reader connector 2nd source	Circuit modify
			Page23: Change mini-card 3V power source from +3VSUS to +3V_S5 for support wake on WLAN from S3/S4 / Change HOLE pad size	Circuit modify
			Page24: Reserve EMI capacitor / add solve insert PCMCIA Card speaker has bo sound circuit	Circuit modify
		20070327	Page25: Add ESD protect circuit	Circuit modify
			Page27: Change MOS footprint	Circuit modify
			Page14: Modify RTC short pad footprint	Circuit modify
			Page17: Modify inductance type	Circuit modify
			Page23: Add capacitors for EMI	Circuit modify
			Page24: Modify FFC connector footprint	Circuit modify
			Page26: Add capacitor for EMI	Circuit modify
			Page27: Reserve EMI circuit	Circuit modify
		20070328	Page22: Delete card reader external EEPROM	Circuit modify
		20070329	Page23: Add pull up resistor on PCIE_WAKE# signal	Circuit modify
			Page18: Delete CMO LED type connector	Circuit modify
			Page25: Reserve ESD protect on kill-switch	Circuit modify
	3B	20070427	Page31: Stuff R/C Snubber for EMI	BOM modify
			Page16: Net BOARD_ID3 change net-name to HOT_KEY and connect ot Page24	Circuit modify
			Page18: Add C561 0.1uF/50V/0603 for EMI Requirement	Circuit modify
			Page23: Add HOLE23 for mechanical requirement	Circuit modify
			Page24: CN5 add a signal "HOT_KEY"connect to Page16 to recognize the Function board is 7 or 3 keys	Circuit modify
			Page25: Add D35 for ESD	Circuit modify
		20070430	Page24: Add D36-D40 for ESD	Circuit modify
		20070509	Page16: Change Board ID Define	BOM modify